

DERWENT-ACC-NO: 1994-134964  
DERWENT-WEEK: 200275  
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TITLE: Integrated circuit packaging system - has grid of  
conductive vias  
through substrate to improve thermal conductivity and  
provide short high  
frequency current path for top side ground plane

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PRIORITY-DATA: 1992US-0938064 (August 31, 1992)

PATENT-FAMILY:

PUB-NO	PAGES	MAIN-IPC	PUB-DATE	LANGUAGE
JP 3335227 B2	004	H01L 023/12	October 15, 2002	N/A
US 5307237 A	007	H05K 007/20	April 26, 1994	N/A
EP 596596 A1	008	H01L 023/538	May 11, 1994	E
JP 06204276 A	004	H01L 021/60	July 22, 1994	N/A
EP 596596 B1	009	H01L 023/538	March 12, 1997	E
DE 69308731 E	000	H01L 023/538	April 17, 1997	N/A

DESIGNATED-STATES: DE FR GB IT DE FR GB IT

CITED-DOCUMENTS: 02Jnl.Ref; EP 63843 ; GB 2118371 ;  
2.Jnl.Ref

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-DESCRIPTOR	APPL-NO
JP 3335227B2	August 31, 1993	N/A	1993JP-0239151
JP 3335227B2	N/A	Previous Publ.	JP 6204276

US 5307237A	N/A	1992US-0938064
August 31, 1992		
EP 596596A1	N/A	1993EP-0306439
August 16, 1993		
JP 06204276A	N/A	1993JP-0239151
August 31, 1993		
EP 596596B1	N/A	1993EP-0306439
August 16, 1993		
DE 69308731E	N/A	1993DE-0608731
August 16, 1993		
DE 69308731E	N/A	1993EP-0306439
August 16, 1993		
DE 69308731E	Based on	EP 596596
N/A		

INT-CL (IPC): H01L021/60; H01L023/12 ; H01L023/538 ;  
H01P005/08 ;  
H05K007/20

ABSTRACTED-PUB-NO: EP 596596B

BASIC-ABSTRACT: The packaging system has an integrated circuit die mounted onto a substrate and has a top side ground plane between the integrated circuit and the substrate, a bottom side ground plane and short high frequency connections between the two ground planes. The top side ground plane decreases signal degradation due to reflections by providing high frequency ground access close to the die and by providing a transmission line for bond wires.

A grid of conductive vias through the substrate improves thermal conductivity and provides the short high frequency current path for the top side ground plane. The die is separated from the top side ground plane by a dielectric layer which also has a conductive layer next the die to provide a back bias voltage.

ADVANTAGE - Reduces signal degradation.

ABSTRACTED-PUB-NO: US 5307237A

EQUIVALENT-ABSTRACTS: An integrated circuit structure comprising: an integrated

circuit die (300) having a back surface and having a plurality of bonding pads arranged on the top surface; a first plurality of wires (324) for electrical ground and a second plurality of wires (318) for electrical signals, wherein each wire from the first plurality of wires and the second plurality of wires is bonded to a corresponding pad in the plurality of bonding pads; a substrate (302) having top and bottom surfaces; a bottom ground plane (306) substantially covering the substrate (302) bottom surface; a top ground plane (308), located on the substrate (302) top surface; a plurality of vias (304) passing through the substrate (302) from the substrate top surface to the substrate bottom surface and connecting said top and bottom ground planes, the vias (304) being electrically and thermally conductive, the vias thereby providing heat transfer from the substrate top surface to the substrate bottom surface and high frequency electrical conductivity from the top ground plane (308) to the bottom ground plane (306); insulation means (310) for insulating the back surface of the integrated circuit die (300) from the top ground plane (308), the insulation means (310) located between the back surface of the integrated circuit die (300) and the top ground plane (308) and being attached to the top ground plane (308); and wherein the top ground plane (308) extends beyond the bottom surface of the integrated circuit die (300), wherein each wire in the first plurality of wires (324) is bonded to the top ground plane (308), thereby providing a short high frequency ground path for each wire in the first plurality of wires (324), and wherein each wire in the second plurality of wires (318) is bonded to signal traces (322) arranged on the substrate top surface beyond the top ground plane, the wires in the second plurality of wires

thus passing near the top ground plane (308), thereby forming a plurality of separate microstrips each composed of a wire in the second plurality of wires (318) in conjunction with the top ground plane (308).

CHOSEN-DRAWING: Dwg.3/4 Dwg.4/4

TITLE-TERMS:

INTEGRATE CIRCUIT PACKAGE SYSTEM GRID CONDUCTING VIAS  
THROUGH SUBSTRATE IMPROVE  
THERMAL CONDUCTING SHORT HIGH FREQUENCY CURRENT PATH TOP  
SIDE GROUND PLANE

DERWENT-CLASS: U11 V04

EPI-CODES: U11-D01A4; U11-D03A2; U11-D03C1; V04-T03;

SECONDARY-ACC-NO:

Non-CPI Secondary Accession Numbers: N1994-106101